REMARKS

The present application was filed on February 16, 2001 with claims 1 through 17. Claims 1 through 17 are presently pending in the above-identified patent application. Claims 8 and 14 are proposed to be cancelled and claims 1, 4-7, 9-11, 13, and 15-17 are proposed to be amended herein.

In the Office Action, the Examiner objected to claims 1-11, 14, and 15 due to indicated informalities and rejected claims 14 and 15 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner also rejected claims 1-3, 5-9, 11-15, and 17 under 35 U.S.C. §102(b) as being anticipated by Kaplinsky (United States Patent Number 5,298,866) and rejected claims 4, 10, and 16 under 35 U.S.C. §103(a) as being unpatentable over Kaplinsky.

The present invention is directed to a method and apparatus for dynamically reducing clock skew among various nodes on an integrated circuit. The disclosed clock skew reduction technique dynamically estimates the clock delay to each node and inserts a corresponding delay for each node such that the clock signals arriving at each node are all in phase with a global clock (or 180° out of phase). Delays attributable to both the wire RC delays and the clock buffer delays are addressed. A feedback path for the clock signal associated with each node allows the round trip travel time of the clock signal to be estimated. When the length of the feedback path matches the length of the primary clock path, the clock skew present at the corresponding node can be estimated as fifty percent (50%) of the round trip delay time. Dynamic adjustments to the delay control circuit are permitted as operating conditions shift. Clock signals arriving at individual nodes on the integrated circuit remain in phase with the global PLL clock (PCK), regardless of variations in the operating voltage or temperature (or both).

The specification has been amended to correct typographical errors.

Formal Objections

Claims 1-11, 14, and 15 were objected to due to indicated informalities. Regarding claims 1 and 6, the Examiner asserts that there is no antecedent basis for the term "the

clock delay" in claim 1, line 3, and claim 6, line 7. Regarding claims 8 and 14, the Examiner asserts that these claims are of improper dependent form for failing to further limit the subject matter of a previous claim. Regarding claims 9 and 15, the Examiner asserts that the term "a primary clock path" refers to the same element as "a primary clock path" in claims 6 and 12, respectively.

Claims 8 and 14 have been cancelled and claims 1, 6, and 12 have been amended to address the Examiner's concerns regarding proper antecedent basis. Applicants, therefore, respectfully request that the objections to claims 1-11, 14, and 15 be withdrawn.

Independent Claims 1, 6 and 12

Independent claims 1, 6, and 12 were rejected under 35 U.S.C. §102(b) as being anticipated by Kaplinsky. Regarding claim 1, the Examiner asserts that Kaplinsky teaches estimating a clock delay for each of said nodes (col. 2, lines 66-67; col. 5, lines 27-28).

Contrary to the Examiner's assertion, Kaplinsky does not *estimate* a clock delay. Kaplinsky teaches "the phase comparator 75 receives the selected return signal on an input 109 and a reference signal REF on an input 111, and *compares* the phase of the two signals." Col. 7, lines 27-30. Thus, since Kaplinsky does not generate an estimate of the delay, the delay device 47 cannot be set to a particular value to compensate for the delay. Instead, Kaplinsky simply determines "which of the two signals leads the other" (i.e., determines the phase difference) and then increases or decreases the delay until "the return signal and reference signal have the same phase." Col. 7, lines 30-36.

Thus, Kaplinsky does not disclose or suggest estimating a clock delay and adjusting said clock signal...based on said estimated clock delay, as required by independent claims 1 and 6, as amended. Similarly, claim 12 includes a "delay driver for adjusting said clock signal...based on an estimated clock delay."

Dependent Claims 2-5, 7-11 and 13-17

Dependent claims 2-3, 5, 7-9, 11, 13-15, and 17 were rejected under 35 U.S.C. §102(b) as being anticipated by Kaplinsky and dependent claims 4, 10, and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kaplinsky.

Claims 2-5, 7-11 and 13-17 are dependent on claims 1, 6, and 12, respectively, and are therefore patentably distinguished over Kaplinsky because of their dependency from amended independent claims 1, 6, and 12 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-17, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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